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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Chin et al.		Confirmation No.:	4508
Serial No. 10/606,258		Art Unit:	2171
Filing Date: June 24, 2003		Examiner:	Usmaan Saeed
Title: METHOD AND SYSTEM FOR MANUFACTURING INTEGRATED CIRCUITS MEETING SPECIAL CUSTOMER REQUIREMENTS WITH MULTIPLE SUBCONTRACTORS IN REMOTE LOCATIONS		Attorney Docket No:	060889-0082-US

PRE-APPEAL BRIEF REQUEST FOR REVIEW

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Commissioner for Patent
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Sir:

This is to request pre-appeal brief review of the rejection of the present application. In the Office Action of November 16, 2006, claims 1-6, 8-13, and 15-20 were rejected under 35 U.S.C. 103(a) as unpatentable over Broberg Patent Application Publication No. 2004/0128641 in view of Atsumi U.S. Patent No. 5,594,639 and Carter et al. (U.S. Patent Application Publication 2003/0074391). Claims 7, 14 and 21 were rejected under 35 U.S.C. 103(a) as unpatentable over these references in further view of pages 354-358 of Sedra/Smith, Microelectronics Circuits (4th ed. 1998). Claims 22-24 were withdrawn as directed to a non-elected invention.

The present invention is directed to a method and apparatus for manufacturing integrated circuits that meet customer specific requirements by using multiple subcontractors in remote locations. In accordance with one embodiment of the invention, customer special requirements received via the Internet are used to update a customer rule set database and the rule set is used to select for further processing physical wafers that are identified in a database and that have

already been partially processed and stored in a die bank. Release requirements are validated against capabilities of the subcontractors and electronic die release orders are issued for release of the selected wafers from the die bank to at least one of the subcontractors for further processing.

The claims of the application have been rejected on a combination of three references, none of which have anything to do with the manufacture of semiconductor integrated circuits: Broberg which is concerned with the design of integrated circuits, Atsumi which relates to general purpose order processing and Carter which relates to the management of equipment and, in particular, oil rigs. It is evident that the rejection has been assembled in hindsight using the framework of the applicants' own invention as a guide. Such a rejection has been expressly prohibited in numerous Federal Circuit decisions.

The primary reference, Broberg, describes a process for the design, not the manufacture, of integrated circuits. This is abundantly clear from the title of Broberg's application, from the preamble to many of his claims and from the description of his invention. While Broberg has a superficial similarity to applicants' invention in that it is responsive to customer requirements (e.g., boxes 520 of Fig. 5 and paragraph 0046), Broberg deals with these requirements at the design stage, not the manufacturing stage. Specifically, as described in paragraph 0029, Broberg uses a suite of generation tools to manage the resources of slice 310 and to enhance productivity. A slice is described at paragraph 0036 as "a partially manufactured semiconductor device in which the wafer layers up to the connectivity layers have been fabricated." However, it must be emphasized that this is the starting point for Bromberg's design effort. Bromberg does not disclose or suggest how he would manufacture the final integrated circuit.

Some of the resource management tools in the generation tool suite are a memory generator, Gen Mem (paragraph 0030), an I/O net list generator (paragraph 0031), a clock generation tool, Gen Clock (paragraph 0032) and a test generation tool, Gen Test (paragraph 0033). Some of the enhancement tools are described in paragraph 0035 as a register and trace generation tool for documenting, implementing and testing registers and internal memories and a tool for configuring spare or unused resources.

Further description of the generation tools is found in Fig. 7 and paragraphs 0054 to 0060. Input to the generation tools includes a series of shells 712, a slice definition 714 and the design or specification of the customer requirements (paragraph 0054). The shells are a

hierarchy of logic enumerated in paragraph 0040 as including register transfer logic (RTL) shells, a documentation shell (paragraph 0049), a verification shell (paragraph 0047), a synthesis shell (paragraph 0048), a static timing analysis shell, a manufacturing test shell, a floor plan shell (paragraph 0050), and an RTL qualification shell. Together the shells and the slice definition comprise an application set.

Paragraph 0055 explains that each tool of the suite of generation tools includes a manager 732, a resource allocation database 734, a resource selector 736 and a composer 738. The resource allocation database 734 appears to be a collection of design elements. As described in paragraph 0056, the resource selectors receive commands from the managers 732 and input from the slice definition 714 and the resource database 734 to build a list of elements to support the requested design. These elements and the customer requirement are forwarded to the composer 738 which generates design views 750 for the requested design in Verilog, VHDL or another design language. The design integrator 782 takes the design views for the requested elements and integrates them into the overall chip design held in the design database 784.

As will be apparent from the foregoing description, Broberg describes a design process, not a manufacturing process.

In contrast, in applicants' invention, customer specific requirements are used to select semiconductor wafers that have already been designed and partially manufactured and the selected wafers are then forwarded on to a subcontractor for further processing.

To emphasize the differences between applicants' invention and Broberg, independent claims 1, 8 and 15 were amended in the response filed August 17, 2006 to emphasize that partially-processed wafers are matched with customer requirements, to describe the assembly capabilities database as storing the capabilities of each subcontractor, and to more fully specify the function of the electronic die release order as providing for release of selected wafers to a subcontractor for further processing.

As amended, claim 1 defines over Broberg at least in specifying the steps of selecting partially-processed wafers identified in a die bank database, validating release requirements against a database of subcontractor capabilities, and issuing orders for release of selected wafers to subcontractors for further processing. None of these steps is disclosed or suggested in Broberg.

Contrary to the Examiner's assertion, Broberg's resource selector 736 does not constitute

or suggest applicants' recited step of selecting partially processed wafers. As emphasized above, resource database 734 appears to be a collection of design elements that are the components of the integrated circuit that is being designed by the generation tool of Fig. 7 and resource selector 736 selects those elements needed for a particular circuit block being designed (paragraph 0056, lines 12-13). Thus, resource selector 736 cannot be said to disclose or suggest the step of selecting partially processed wafers from a die bank as recited in applicants' claims.

The Examiner concedes that Broberg does not teach the claimed elements of validating special release requirements for selected dies or issuing electronic die release orders but maintains that Atsumi makes up for those deficiencies. Applicants respectfully disagree. Atsumi merely describes an order processing module that breaks down orders into component parts. He makes no mention of processing electronic components of any sort and no mention of further processing of semiconductor wafers. In particular, he does not suggest applicants' invention in which partially processed wafers are selected from a die bank in accordance with customer specifications and then released for further processing in accordance with the capabilities of available subcontractors.

Nor is there any suggestion in the Broberg and Atsumi references to combine these references in a way that would suggest applicants' invention. In the first place, the references come from two completely unrelated fields: integrated circuit design and order processing. A person skilled in the art of integrated circuit design is not trained in order processing and one skilled in order processing is not trained in integrated circuit design. Integrated circuit design is a discipline of electrical engineering. Order processing of the type described by Atsumi appears to be a discipline of business planning. One skilled in electrical engineering is not likely to look to business planning for solutions to his problems and one skilled in business planning is not likely to look to electrical engineering for solutions to his problems. Accordingly, there is no incentive to combine the teaching of these two references.

Moreover, even if the references were combined they still would not suggest the claimed invention. In particular, neither Broberg nor Atsumi suggests a manufacturing process as claimed where partially-processed physical wafers are selected form a die bank in accordance with customer requirements and release requirements are validated in a subcontractor's assembly capability database so as to issue die release orders for release of selected wafers for further processing by a subcontractor.

Moreover, it is respectfully submitted that Carter does not make up for these deficiencies. Carter describes in Fig. 55 a system for calculating economic day rates for drilling equipment. Again, the Carter reference is from a technology field—oil well drilling—far removed from the diverse technologies of Broberg and Atsumi. Again, one skilled in petroleum drilling technology is not likely to have any training in the integrated circuit design or order processing technologies of Broberg and Atsumi; and vice versa. Thus, there is again no incentive to combine the references.

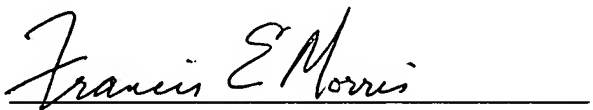
And even if combined, the references still do not suggest applicants' claimed invention. While Carter illustrates a database 5580 of rig and contractor capabilities in Fig. 55, he does not describe the database and apparently uses it only for price computations. Most importantly, Carter does not make up for the deficiencies of Broberg and Atsumi. He does not suggest a method of manufacturing semiconductor wafers and he does not suggest a method in which partially-processed wafers are selected from a die database in accordance with customer specifications, release requirements are validated in accordance with subcontractor capabilities and selected wafers are released to a subcontractor for further processing.

For the foregoing reasons, it is respectfully submitted that claim 1 is patentable over the references applied. Independent claims 8 and 15 are believed patentable for the same reasons claim 1 is patentable. Dependent claims 2-7, 9-14 and 16-21 are believed patentable for the same reasons the independent claims are patentable. In addition, the dependent claims are believed patentable for the additional reason that they specify further details of the wafer selection process and wafer manufacturing process, neither of which are addressed in the references which do not describe wafer selection or wafer manufacturing..

In view of the foregoing remarks, the claims in this application are believed to be in condition for allowance. Such action is respectfully requested.

Respectfully submitted,

Date: May 16, 2007



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